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ASICs, power circuits,
education, active cooling

ASICs DESIGN – EDUCATION AND RESEARCH

The paper presents some research topics and computer programs for education, which were developed in the Microsystems Design Group of the Institute of Electronics AGH (http://scalak.elektro.agh.edu.pl/).

1. INTRODUCTION

The paper deals with some examples of education and research projects carried out at ASICs (Application Specific Integrated Circuits) area in the Microsystems Design Group (MDG) of the Institute of Electronics AGH. Our ASICs laboratory is fully equipped with software and hardware for professional designs. A lot of students' projects prove that the designing is simple and accessible by every engineer working in the microelectronics field. The research carried out at the MDG can be divided into three main branches: thermal problems in microcircuits, optimum topography design and testing, artificial neural networks application to microelectronics. Some designs have been already fabricated in the CMOS process.

2. EXEMPLARY PROGRAMS FOR EDUCATION.

The program HORSON was created for optimal placement of heat sources of a microcircuit. It leads to regular temperature distribution on the substrate. The program uses a heuristic method described in [1]. The method matches up appropriate areas with each power source and places the sources into the centres of gravity of the areas. The placement is quasi-optimal. The input data (values of power) for HORSON come as a result of circuit analysis by SMASH. The quasi-optimal topography generated by this program is verified by another program called HEATANALISER. Figure 1 presents co-operation of these programs. Figure 2 shows areas corresponding to values of powers dissipated in each heat source (result of HORSON). Figure 3 presents temperature distribution on the chip as an effect of HEATANALISER.

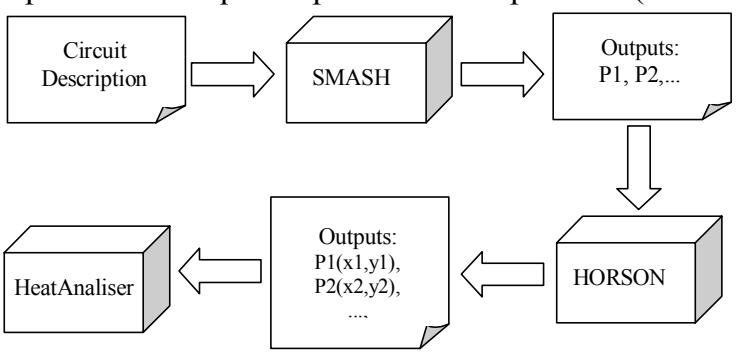

Fig. 1. Co-operation of programs.

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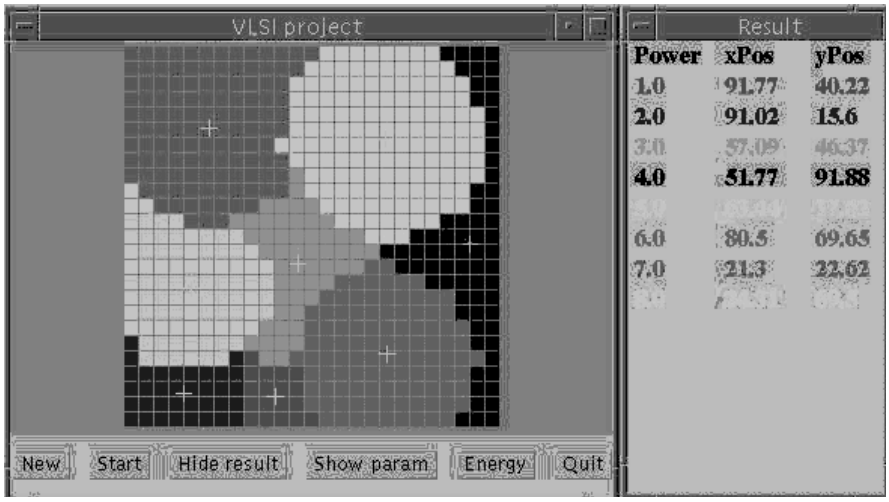

Fig. 2. Result of HORSON partitioning.

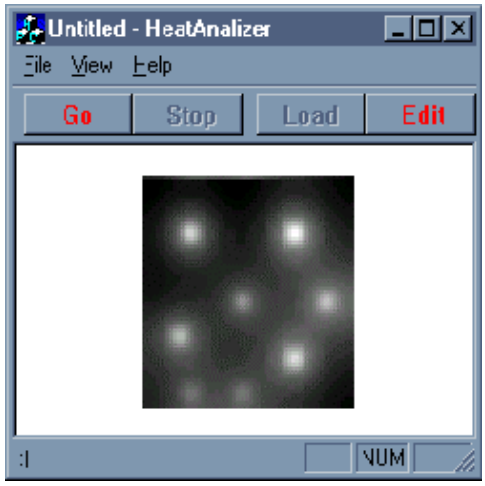

Fig. 3. Temperature distribution on the substrate.

Another program called TOPOGRAD devoted to thermal optimisation of the chip topography utilises gradient methods [2]. The program has got a user-friendly graphic interface. The editor defines the lateral dimensions of the chip, scale, values of power, convection coefficient and grid. Thermally significant components are pointed out with a computer mouse. As a result of the execution of the program an optimum topography and values of temperature of the power components are obtained. The example of the program action is presented in Fig. 4 and Fig. 5.

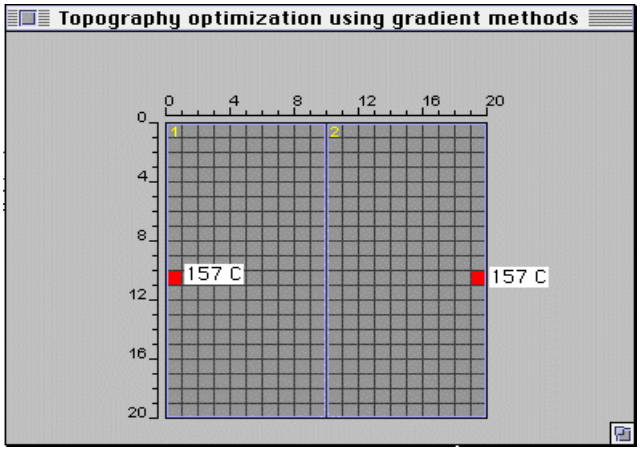

Fig. 4. Example – start point before optimisation

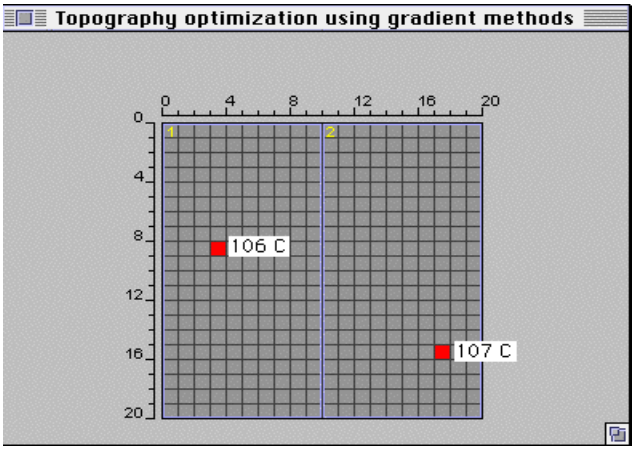

Fig. 5. Optimum placement – after optimisation

SHORTPATH is one of the programs for topography optimisation taking into consideration the total length of interconnections between components. The algorithm is based on λ-optimal solution method [3]. The first part of the program generates a starting solution (Best-Match method and random placement of components) and then the solution is corrected (2- or 3-optimal method or mixed both methods). A user defines connectivity matrix, dimensions of a chip and chooses the method of solution.

HEATCON is a tool for complex optimisation of the topography of a chip. At the beginning the program optimises the total length of interconnections and later on it minimises temperatures of the components. The algorithm utilises Kohenen networks. A user decides which criterion (temperature or total length of connections) has bigger priority.

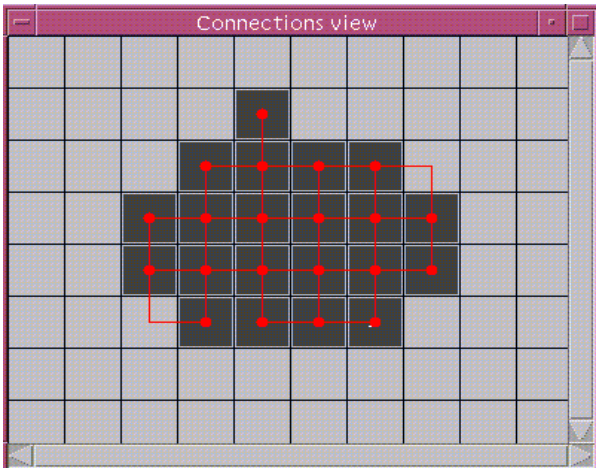

Fig. 6. Component placement with SHORTPATH .

3. ASICs DESIGNS.

The layout of the analogue controller for car ignition system [4] is presented in Fig. 7.

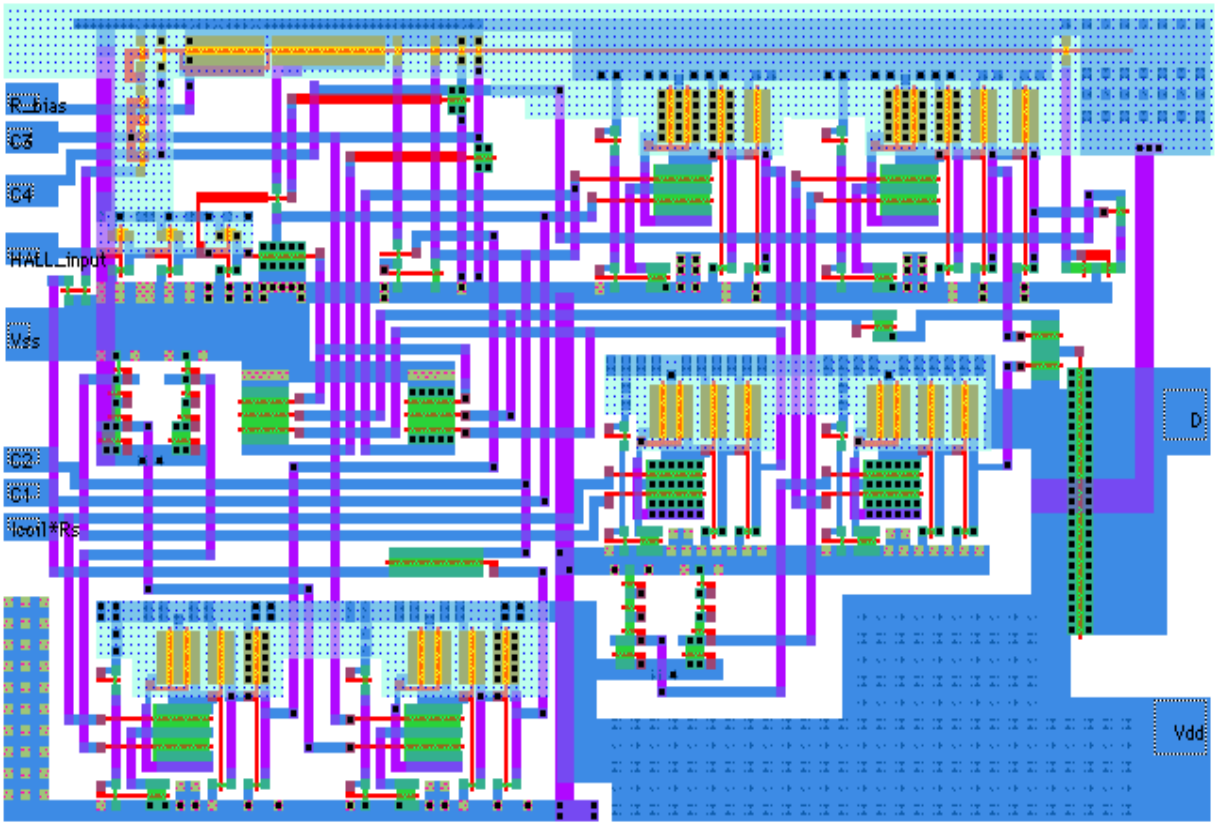

Fig. 7. Controller for car ignition system.

The controller possess some unique features necessary for modern car ignition systems. It uses a Hall device as a sensor of rotation speed. The controller drives coil current providing the required stored energy with low dissipation. All blocks of the layout were designed as a full-custom cells using IMIOCAD software (layer editor: UNCLE [5] and layer extractor: EXCES [6]).

The layout of 8-bit full adder is shown in Fig. 8. It is an example of students' designs.

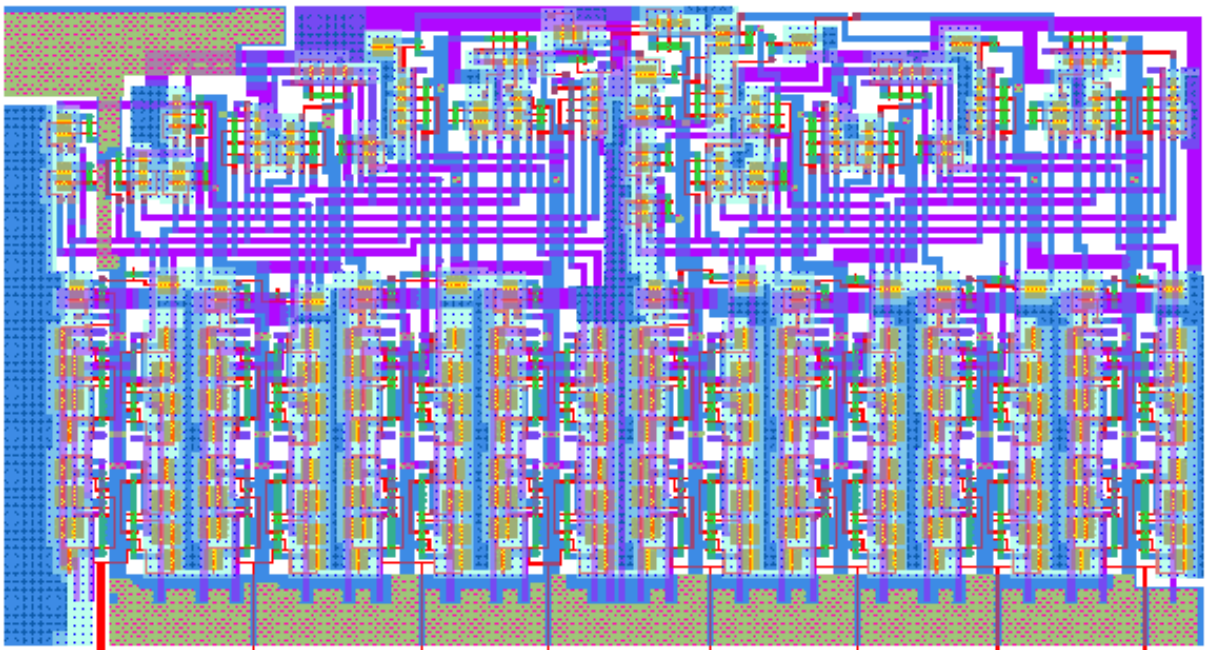

Fig. 8. 8-bit adder. Students' design.

Figure 9 presents a layout of the test ASIC for active cooling of power ICs [7].

A special ASIC was designed to control the active heat sink with a Peltier heat pump according to power consumption or temperature changes in a cooled chip. Various kinds of cooling of ICs were tested. The ASIC could be used as a standard cell in VLSI circuits to control the thermal resistance between a chip and an ambient to minimise the energy supplying the Peltier pump and to keep the structure under the temperature limit.

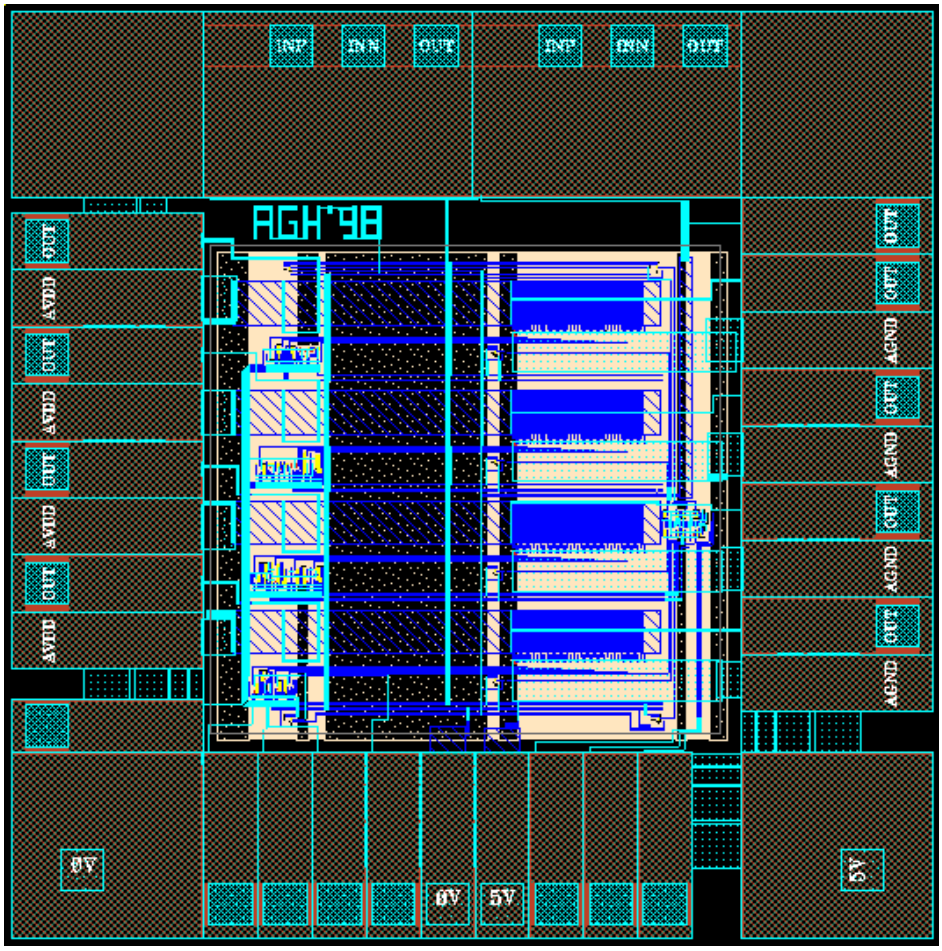

Fig. 9. Test ASIC for active cooling of power ICs.

4. CONCLUSIONS

The paper presents some examples of research and teaching activities on the VLSI circuits area in the Institute of Electronics AGH.

5. ACKNOWLEDGEMENTS

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